Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 6 and 11 have been amended. No claims have been cancelled. Therefore, claims 1, 4-6, 9-11, and 14-21 are presented for examination.

Claims 1, 4-6, 9-11 and 14-21 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants submit that claims 1, 6 and 11 have been amended to appear in proper condition for allowance.

Claims 1, 4-6, 9-11 and 14-21 stand rejected under 35 U.S.C. §102(e) as being anticipated by Rozas (U.S. Patent No. 6,725,361). Applicants submit that the present claims are patentable over Rozas.

Rozas discloses that in order to eliminate the wait for the FTEN instruction to execute at the end of a first sequence of translated instructions, the improved invention instead assumes what the top-of-stack will be at the end of the first sequence and translates the following sequence of instructions using this assumed value. The assumed value for top-of-stack is retained as a part of context so that it may be compared with an actual value for top-of-stack after completion of the preceding sequence of translated instructions. A translation is generated using the assumed value. Before the succeeding translation is executed, the actual top-of-stack determined by the translation software at the completion of the preceding sequence is compared to the assumed value. If the values are the same, the succeeding translation is executed. If the values differ, the operation of the processor is rolled back to state existing at the beginning of the translation; and a new translation is utilized. See Rozas at col. 8, ll. 64 – col. 9, ll. 18.

Claim 1 of the present application recites:

A method of translating instructions, said method comprising:

translating a first block of instructions executable in a first processor architecture into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions;

during the translating, generating an expected Top of Stack (TOS) position in said stack for said first block of instructions;

during the translating, adding at least one instruction to said translated first block of instructions to determine if a first expected TOS is equal to an actual TOS position in said stack at a time of executing said translated first block of instructions; and

executing said translated first block of instructions without restarting the translating, wherein during the executing said at least one instruction to branch to correction code if said expected TOS is not equal to said actual TOS, said correction code to generate a delta of said expected TOS and said actual TOS and to adjust said stack for said first block of instructions by said delta at the time of executing said translated first block of instructions;

wherein said translated first block of instructions to continue executing after said at least one instruction adjusts said stack.

Applicants submit that Rozas does not disclose executing a translated first block of instructions without restarting translating, wherein during the executing at least one instruction to branch to correction code if an expected TOS is not equal to an actual TOS. Rozas clearly discloses that ***before*** a succeeding translation is executed, an actual TOS determined by translation software at the completion of a preceding sequence is compared to an assumed value. Further, Rozas discloses that if the TOS values are the same, the translation is executed, but if different the operation of the processor is rolled back to state existing at the beginning of the translation. Thus, it is apparent that Rozas does not disclose a process ***during execution*** *where an* ***instruction branches to correction code*** *if an expected TOS is not equal to an actual TOS*, since Rozas discloses examining expected TOS and actual TOS **during the translation by translation software**. Therefore, claim 1 is patentable over Rozas. The fact that this process occurs during translation, and not during

execution of a translated instruction, is supported by Rozas at col. 9, ll. 19-23 where it is disclosed that such an improvement in the invention eliminates the need to execute a FTEN instruction at the ***end of a translated sequence of instructions***.

Independent claims 6 and 11 also recite executing a translated first block of instructions without restarting a translating, wherein during the executing at least one instruction to branch to correction code if an expected TOS is not equal to an actual TOS, the correction code to generate a delta of the expected TOS and the actual TOS and to adjust a stack for the first block of instructions by the delta at the time of executing the translated first block of instructions, wherein the translated first block of instructions to continue executing after the at least one instruction adjusts the stack. Therefore, claims 6 and 11, as well as their respective dependent claims, are patentable over Rozas for the reasons discussed above with respect to claim 1.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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Date: 3/12/07

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